PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : H01L 21/44, 29/00

A1

(11) International Publication Number: WO 00/35000

(43) International Publication Date: 15 June 2000 (15.06.00)

(21) International Application Number: PCT/US99/28955

(22) International Filing Date: 8 December 1999 (08.12.99)

(30) Priority Data:
09/207,906 8 December 1998 (08.12.98) US

(71) Applicant: CVC PRODUCTS, INC. [US/US]; 525 Lee Road, Rochester, NY 14603 (US).

(72) Inventor: MOSLEHI, Mehrdad, M.; 956 Stanley Avenue, Los Altos, CA 94024 (US).

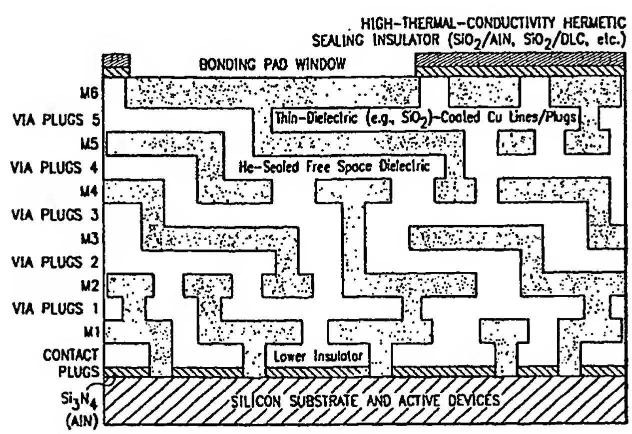
(74) Agent: SPRINKLE, Steven, R.; Gray Cary Ware & Freidenrich, Suite 1440, 100 Congress Avenue, Austin, TX 78701 (US).

(81) Designated States: DE, GB, JP, KR.

Published

With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: ULTRA HIGH-SPEED SEMICONDUCTOR INTEGRATED CIRCUIT INTERCONNECT STRUCTURE AND FABRICATION METHOD USING FREE-SPACE DIELECTRIC



(57) Abstract

Ultra high-speed multi-level interconnect structure and fabrication process flows are disclosed for a semiconductor integrated circuit chip. The interconnect structure includes a plurality of conductive metallization levels (M1 – M5). Each of the metallization levels includes a plurality of conductive interconnect lines. A plurality of conductive plugs (via plugs 1 – via plugs 5) make electrical connections between various metallization levels as well as between the metallization levels and the semiconductor devices fabricated on the semiconductor substrate. The interconnect lines and plugs are at least partially surrounded by a free-space medium and are formed using an electrically conducting or semi-conducting disposable filler material that can be removed using a dry etch process. A top passivation overlayer hermetically seals the multi-level interconnect structure.

ULTRA HIGH-SPEED SEMICONDUCTOR INTEGRATED CIRCUIT INTERCONNECT STRUCTURE AND FABRICATION METHOD USING FREE-SPACE DIELECTRIC

FIELD OF THE INVENTION

The present invention relates to semiconductor integrated circuits and, more particularly, to structures and methods of fabricating integrated circuit interconnect devices. Even more particularly, the present invention relates to an improved method of forming such an interconnect structure that integrates free-space intermetal and interlevel dielectric regions with at least one high-conductivity interconnect conductor. This invention offers an improved interconnect structures and method of forming same which will reduce semiconductor device damage during back-end processing caused by the plasma charging effect.

BACKGROUND OF THE INVENTION

The speed and reliability performance parameters of state-of-the art semiconductor integrated circuit (IC) chips are mostly governed by the on-chip interconnects. Advanced semiconductor IC chips employ multi-level on-chip interconnects usually comprising aluminum (usually an alloy of aluminum comprising approximately 0.5% to 2% copper for improved electromigration reliability lifetime) metal lines, aluminum (again typically doped with copper) or tungsten plugs (for inter-level/inter-metal contact/via holes), and silicon dioxide (or fluorinated silicon dioxide SiO_xF_y) or a combination of silicon dioxide with an organic

low-permittivity (low-k) dielectric used as inter-metal and inter-level dielectrics. The speed performance of advanced semiconductor IC chips such as high-end microprocessors and digital signal processors (DSP) fabricated using 0.25 μm complementary metal-oxide-semiconductor (CMOS) technologies and beyond is limited by the interconnect signal propagation delays. The signal propagation delay for advanced interconnects is limited by the parasitic resistive, capacitive, and inductive elements. These include the interconnect metal "RC" delays, capacitive cross-talks or cross-talk noise between adjacent metal lines (due to voltage pulses), as well as inductive noise and cross-talks (due to voltage pulses).

As the device dimensions are scaled down, the metal interconnect line widths and pitches are also scaled down, accordingly. The maximum density (areal density) of metal interconnect lines on each interconnect level is limited by the minimum electrical conductivity requirements of the metal lines as well as the upper limits on the maximum allowable signal cross-talks. As the density of the metal interconnect lines on each interconnect level increases, the adjacent metal lines are placed closer to each other and the widths of the metal lines is also reduced. As the minimum feature size of the semiconductor (e.g., silicon CMOS) IC technologies is reduced to 0.25 μm and beyond, the "RC" propagation delays and the capacitive cross-talk noise have a significant impact on the speed performance of the IC chips, such as in high-end microprocessor and digital signal processor (DSP) chips. These problems place serious constraints on the minimum width (and thickness) of the

metal lines and the minimum metallization layout pitches (or the minimum inter-line spacings), particularly on the interconnect levels which contain the long-range global interconnect lines (for instance, for signal or clock distribution) and/or power distribution.

The interconnect design rule constraints caused by the IC chip speed performance (and electromigration reliability lifetime) requirements result in an increase in the number of interconnect levels, particularly for complex logic chips such as high-end/high-speed microprocessors and digital signal processors. For instance, state-of-the-art CMOS logic technologies with minimum feature size of 0.20 to 0.25 μm may utilize as many as six or more levels of metal interconnects. Each additional level of metal interconnect adds significantly to the overall process flow complexity and chip manufacturing cost. This is due to both increased number of fabrication process steps in the process flow and the manufacturing yield reduction associated with a more complex and lengthy process flow.

Another limitation associating with existing interconnect structures arises because metal resistivity significantly contributes to the chip speed constraints and even the overall manufacture cost. The use of a higher conductivity metal such as copper instead of aluminum, since the bulk resistivity of copper is approximately 1.78 μΩ•cm versus approximately 2.7 μΩ•cm for aluminum, results in a significant reduction of the interconnect "RC" propagation delay for a given metal interconnect width and thickness. On the other hand, for a given interconnect line parasitic resistance, a higher metal conductivity

(e.g., Cu instead of Al) allows the use of thinner metal lines on each interconnect level for a given metal line width. This, in turn, enables closer spacings between the adjacent metal lines or equivalently, a higher areal density of metal interconnect lines on each level for a given distribution of intra-level capacitive signal cross-talks.

The higher interconnect line densities on various interconnect levels enable a reduction in the number of required interconnect levels for a given chip speed performance. This results in reduced process complexity and cost. Alternatively, a higher conductivity conductor (e.g., copper instead of Al) can be used to not only reduce the process complexity and cost through reduction of the number of interconnect levels, but also to improve the chip speed performance. This can be done by both reducing the metal line resistance, increasing the interconnect metal line resistance, and increasing the interconnect metal line areal density.

For example, in an advanced 0.18 μm microprocessor logic chip, for a given maximum speed or clock frequency (e.g., an approximately 600-MHz microprocessor), comprising eight levels of Al metal interconnects, replacing Al with Cu accomplishes a number of desirable results. For instance, it is possible to reduce the process complexity and chip fabrication cost by, perhaps, approximately 30% while achieving the same speed performance of approximately 600 MHz. This can be achieved by reducing the number of interconnect levels from 8 to 6 and also due to the reduced number of process steps per level for copper interconnect

compared to aluminum interconnect. It is also be possible to reduce the process complexity and chip fabrication cost by, perhaps, approximately 15-20%, while also improving the chip speed performance by, for instance, approximately 10% to approximately 660 MHz. For example, this may be achieved by reducing the number of metal interconnect levels from 8 to 7 and also reducing the resistance of the metal lines at the same time.

Besides the interconnect metal, the inter-metal/inter-level dielectric layers (IMD and ILD layers) also have a significant impact on the IC chip performance speed as well as manufacturing cost. The dielectric constant (i.e. relative dielectric constants with respect to free space) of the IMD/ILD material layers impacts not only the "RC" propagation delays but also the intra-level and inter-level capacitive cross-talks.

The mainstream ILD/IMD materials in silicon chip manufacturing are silicon dioxide (SiO_2) and/or derivatives of silicon dioxide (such as fluorinated silicon dioxide: SiO_xF_y) with k values in the range of 3.2 to over 4.0. There has been a significant amount of materials research on low-k dielectrics. The lowest practical k values to date have been reported for some spin-on organic dielectrics and porous aerogels/xerogels. The practical low-k dielectrics developed to date have k values in the range of 2.0 to 3.2. These low-k dielectrics, however, complicate the back-end interconnect process integration due to their inferior thermal stability as well as their electrical, mechanical and thermal conductivity properties compared to silicon dioxide.

FIGURE 1 illustrates a side view of an interconnect structure 10 that includes a low-k organic ILD/IMD material layer 12 and trench 14. SiO_2 layer 16 covers ILD/ILD substrate 12. Covering trench 14 and top SiO_2 layer 16 is conformal SiO_2 buffer layer 18. The formation of organic low-k dielectric layer 12 also complicate the single or dual damascene processes commonly used for fabrication of copper interconnects due to the difficulties associated with their incompatibility with chemical-mechanical polishing (or CMP) processes used for copper and barrier removal during the interconnect fabrication process. As a result, most organic low-k dielectrics employ a suitable hard mask layer such as silicon dioxide for single or dual-damascene interconnect fabrication processes in order to facilitate formation of dielectric trenches and via holes for the embedded (inlaid) metal (e.g., copper) lines.

The optimal integration of most organic low-k dielectrics requires deposition of a thin conformal layer of, for instance, silicon dioxide, such as SiO_2 layer 18, followed by an anisotropic oxide etch process in order to cover the trench and via hold sidewalks with a thin layer of high-quality silicon dioxide dielectric, such as SiO_2 layer 18. This prevents a direct contact between the low-k dielectric and the deposited glue/barrier layer and may improve the overall breakdown voltage and leakage characteristics of the composite ILD/IMD layers. This requirement adds to the complexity and fabrication cost of the IMD/ILD integration. Moreover, the effective relative dielectric constant of the composite IMD/ILD layers is somewhat higher than that of the low-k dielectric by

itself. This is due to the requirements for the hard mask and sidewalk oxide coverage.

The prior art multi-level interconnect structures (using either silicon dioxide or any solid ILD/IMD low-k material layer) typically require an effective glue/barrier layers. This is particularly critical for a high electrical conductivity material such as copper (or silver) since copper (or silver or gold) act as electrical trap centers in silicon and can severely degrade the transistor properties such as transconductance, junction leakage, standby power dissipation and reliability lifetime. Moreover, copper, as well as some other metallic elements such as gold and silver can cause severe degradation of the ILD/IMD layers adversely affecting their electrical leakage and breakdown properties. As a result, the prior art silicon chip interconnect structures and fabrication process flows employ conductive diffusion barrier layers (such as TiN, Ta, TaN, TiSiN, TaSiN, WN, WSiN, MoN, or MoSiN). The long-term chip reliability lifetime and chip manufacturing yield requirements place limits on the minimum thickness of the barrier material for such devices.

As the chip IC device dimension are scaled down, the width of the metal lines and also the dimensions or diameters of the via plugs are also reduced, whereas the thickness of the diffusion barrier layer is scaled down more slowly. Thus, with each successive technology generation, the barrier material thickness (and cross sectional area) becomes a larger fraction of the conductive interconnect lines. One example of this phenomenon can be examined in the case of dual-damascene copper

interconnects. In IC chips with copper metallization, a larger fraction of the diameter of the conductive via plug is also consumed by the barrier material. For instance, for a damascene trench width of 0.20 µm and a conformal diffusion barrier thickness of 250 Å (deposited, for example, by a conformal chemical-vapor deposition or CVD process), the high-conductivity metal (e.g., copper with a resistivity of approximately 1.8 µΩ•cm) only occupies a metal line width or a via plug diameter of only 0.15 µm, due to the peripheral space occupied by the diffusion barrier layer. Since the typical diffusion barrier layers have much higher electrical resistivity values compared to the high-conductivity interconnect metals (e.g., in the range of approximately 150-250 µΩ•cm for Ta and TaN diffusion barriers vs. approximately 1.8 µΩ•cm for copper), the diffusion barrier layer degrades the overall interconnect metal line resistance, as well as via plug resistance values. For instance, FIGURE 2 shows damascene dielectric trench structures 20 and 22 (e.g., for fabrication of embedded copper metal line) with a width W and height H.

In damascene dielectric trench structure 22 (Fig. 2b), trench 24 is filled entirely with the high conductivity metal line having electrical resistivity of ρ_m. On the other hand, damascene trench structure 20 (Fig. 2a) includes barrier layer 26 (shown as a conformal layer) with a layer thickness t_b and a material resistivity of ρ_b in trench 28. The high conductivity metal line 28 occupies the remaining space surrounded by the barrier layer.

Assuming $\rho_b >> \rho_m$, which is typically the case in practice, we can compare the total conductor line resistance per unit length for these two conditions:

$R_1 \triangleq$ conductor line resistance per unit length without the barrier layer (Fig. 2b);

$R_2 \triangleq$ conductor line resistance per unit length with the barrier layer (Fig. 2a)

$$R_1 = \frac{\rho m}{W \cdot H}, \quad R_2 = \underbrace{\overbrace{\left[\frac{Pm}{\left(W-2t_b\right)\left(H-t_b\right)}\right]}^{R2m} \Bigg\| \overbrace{\left[\frac{Pb}{t_b\left(2H+W\right)}\right]}^{R2b}}_{\text{Two resistive components in parallel}}$$

Since $\rho_b >> \rho_m$, the conclusion follows that $R_{2b} >> R_{2m}$ and, as a result, $R_2 \cong R_{2m} = \dfrac{\rho m}{\left(W-2t_b\right)\left(H-t_b\right)}$

$$R_2 \cong \frac{\rho m}{WH + 2t_b^2 - t_b W - 2t_b H}$$

$$R_2 \cong \frac{\rho m}{WH - t_b\left(W+2H\right) + 2t_b^2}$$

$$\therefore \frac{1}{R_2} \cong \frac{WH + 2t_b^2 - t_b\left(W+2H\right)}{\rho m}$$

$$\frac{1}{R_2} = \frac{WH}{\rho m} + \frac{2t_b^2 - t_b\left(W+2H\right)}{\rho m}$$

$$\frac{1}{R_2} \cong \frac{1}{R_1} - \left[\frac{t_b\left(W+2H-2t_b\right)}{\rho m}\right]$$

For instance, assume W=0.25 µm, H=0.50 µm, t_b=250 Å (0.025 µm), and Pm ≅ 2 $\mu\Omega$•cm:

$$R_1 = \frac{\rho m}{W \cdot H} = \frac{2x10^{-6}\Omega \bullet cm}{(0.25x10^{-4}\,cm)(0.50x10^{-4}\,cm)}$$

$R_1 = 1600\,\Omega/cm$ (without barrier)

$$R_2 \cong \frac{2x10^{-6}\Omega \bullet cm}{(0.25-0.05)(0.50-0.025)x10^{-8}} = \frac{200}{0.20x0.475}\Omega/cm$$

$R_2 = \frac{1000}{0.475}$ Ω/cm ≅ 2105 Ω/cm with barrier

$R_1 = 1600$m Ω/cm, R_2 ≅ Ω/cm

As a result, in this example, the presence of the barrier layer has degraded the effective interconnect line resistance by over 30% which is a significant amount of interconnect conductor conductivity loss.

Similarly, the barrier layer can also degrade the effective via plug resistance. For instance, FIGURE 3 shows via plugs 30 and 32 connecting the metal lines between two adjacent interconnect levels. Via plug 30 (Fig. 3a) includes metal plug between metal lines 34 and 35 which is fully surrounded at the bottom and sidewalls by the barrier layer 36. Via plug 32 of Fig. 3b, on the other hand, shows an ideal situation without a barrier layer surrounding metal plug 32 (connecting metal lines 38 and 40).

Assume the via hole (cylindrical via hole) has a diameter of D and a height of H. We can also define the following parameters:

R_{p_2} ≙ effective via plug resistance with the barrier layer (Fig. 3a); and

R_{p_1} ≙ effective via plug resistance without the barrier layer (Fig. 3b).

Also, assume that the via plug metal has a resistivity of ρ_m (1.8 μ•cm), which is preferably the same as that of the interconnect metal lines on levels N and N-1). Moreover, assume that the barrier layer is conformal, has a thickness of t_b, and a resistivity of ρ_b. Moreover, assume that $\rho_b >> \rho_m$. Let's calculate R_{p_1} and R_{p_2} for the two via plug structures of Figs. 3a and 3b:

$$R_{p_1} = \frac{\rho_m H}{\left(\frac{\Pi D^2}{4}\right)} = \frac{4\rho_m H}{\Pi D^2}$$

$$R_{p_2} \cong \underbrace{\left\{\frac{\rho_m(H-t_b)}{\left[\frac{\Pi(D-2t_b)^2}{4}\right]}\right\} \Bigg\| \frac{\rho_b(H-t_b)}{\left\{\frac{\Pi}{4}\left[D^2-(D-2t_b)^2\right]\right\}}}_{\text{two resistive components in parallel}} + 2Rc + \frac{\rho_b t_b}{\left(\frac{\Pi D^2}{4}\right)}$$

Since ρb>>ρm

$$R_{p_2} \cong \frac{4\rho_m(H-t_b)}{\Pi(D-2t_b)^2} + \frac{4\rho_b t_b}{\Pi D^2} + 2Rc$$

Where Rc is the effective contact resistance at each interface between the barrier layer and either the via metal plug or the underlying metal line. As an example,

assume D=0.25 μm, H=0.75 μm, t_b=250 Å (0.025 μm), and $P_m \cong 2$ μΩ•cm ($\rho_b >> \rho_m$). Assume that $\rho_b \cong 200\mu\Omega$•m. R_{p_1} and R_{p_2} can be calculated as follows:

$$R_{p_1} = \frac{4x2x10^{-6}\,\Omega\bullet\mathrm{cm}\;x\;0.75x10^{-4}\,\mathrm{cm}}{\Pi\left(0.25x10^{-4}\,\mathrm{cm}\right)^2}$$

$$= \frac{6x10^{-10}\Omega\;\mathrm{cm}^2}{\Pi\,x\;0.25^2\;x\;10^{-8}\;\mathrm{cm}^2} = \frac{96x10^{-2}}{\Pi}\Omega \cong 0.305\;\Omega$$

Thus, $R_{p_1} \cong 0.305\Omega$ which is the plug resistance for the ideal case without the barrier layer.

$$R_{p_2} \cong \frac{4\;x\;2\;x\;10^{-6}(0.75-0.025)\;x\;10^{-4}\;\;\Omega\bullet\mathrm{cm}^2}{\Pi\left[(0.25-2\;x\;0.025)\;x\;10^{-4}\right]^2\;\mathrm{cm}^2}$$

$$+\frac{4\;x\;200\;x\;10^{-6}\;\;x\;0.025\;x\;10^{-4}\;\;\Omega\bullet\mathrm{cm}^2}{\Pi\left(0.25\;x\;10^{-4}\right)^2\;\mathrm{cm}^2}+2Rc$$

$$= \frac{8\;x\;0.725\;x\;10^{-10}}{\Pi\,x\;0.20^2\;\;x\;10^{-8}} + \frac{2\;x\;10^{-9}}{\Pi\,x\;0.25^2\;\;x\;10^{-8}} + 2Rc\;\Omega$$

$$R_{p_2} = \frac{5.8\;x\;10^{-2}}{\Pi\,x\;0.040} + \frac{2\;x\;10^{-1}}{\Pi\,x\;0.25^2} + 2Rc\;\Omega = 0.462 + 1.019 + 2Rc\;\Omega$$

Thus, $R_{p_z} = 1.480 + 2Rc\,\Omega$, which is the plug resistance for the via plug structure comprising the barrier layer.

It can be seen that even without including the contact resistance contribution 2Rc (due to the two barrier/metal contact interfaces in each plug), the barrier layer results in a significant degradation of the overall via plug resistance. This effect, in turn results in the

degradation of the chip speed due to the increased "RC" propagation delays in the interconnect structure.

In light of the above information, therefore, there is need for a semiconductor IC chip interconnect structure and a related fabrication process flow which can significantly reduce the parasitic resistive and capacitive elements, as well as the related "RC" propagation delays and interconnect capacitive cross-talks. Satisfying this need will enable much faster chip operations and/or lower chip power consumption.

Moreover, there is a need for an improved chip interconnect structure and related process flow which can enable a reduction of the total number of on-chip interconnect levels required for fabrication of high performance semiconductor IC chips. Satisfying this need results in a reduction in the chip fabrication process flow complexity, improving the manufacturing yield, and reducing the overall production costs.

There is the need for an interconnect structure and a related interconnect fabrication process flow which enable the use of a lowest possible dielectric permittivity for IMD/ILD applications.

One attempt to provide a lowest possible relative permittivity or k value has been to use free space dielectric between interconnects. Free space provides the best possible dielectric since it provides k = 1. This is a factor of approximately 4 times better than silicon dioxide and even a factor of 2 to 3 better than the best practical low-k dielectric materials. As a result, for a given metal conductivity and sheet resistance distribution,

the free-space dielectric results in a significant reduction of the interconnect "RC" propagation delays and capacitive cross-talk noise.

One of the main challenges with the free-space dielectric IMD/ILD integration is the ability to prevent damage to the multi-level interconnect structure and underlying devices during etching of the metal transfer and during etching of the via and contact holes. At the end-point, the plasma can charge the interconnect structure and cause damage to the underlying device(s). This charging effect can be magnified by the "antenna effect".

There is a further need for an interconnect structure and related fabrication process flow that can eliminate the additional process complexities and fabrication cost associated with the integration of low-k dielectric materials by using free-space as the IMD/ILD layers. There is also a need for an advanced multi-level interconnect structure and a related fabrication process flow which enable efficient heat removal from the interconnect structure, and also allow formation of a fully hermetically sealed chip package.

SUMMARY OF THE INVENTION:

In accordance with the present invention, an ultra-high-speed semiconductor IC chip interconnect comprising free-space dielectric medium is disclosed that substantially eliminates or reduces disadvantages and problems associated with previously developed and prior art multi-level interconnect structures and methods of fabrication.

According to one embodiment of the present invention, an ultra-high-speed multi-level chip interconnect structure is provided for a semiconductor IC chip that includes a plurality of electrically conductive metallization levels. Each of the metallization levels includes a plurality of electrically conductive interconnect lines or segments. A plurality of electrically conductive via and contact plugs make electrical connections between various metallization levels as well as between the metallization levels and the semiconductor devices. The invention further includes a free-space medium occupying at least a substantial fraction of the electrically insulating regions separating the conducting lines and plugs within the multi-level interconnect structure. A top passivation overlayer hermetically seals the multi-level interconnect structure and the underlying devices on the semiconductor substrate. The top passivation overlayer also functions as an effective heat transfer medium to facilitate heat removal from the interconnect structure as well as an additional mechanical support for the interconnect structure through a sealing contact with the top metallization level of the multi-level interconnect structure.

A technical advantage that the present invention provides is the practical use of a free-space interlevel/intermetal (ILD/IMD) dielectric medium. With the present invention, the interconnect structure provides reduced "RC" propagation delay and reduced capacitive cross-talk.

For an N-level ($N \geq 1$) interconnect structure, the present invention also provides the additional technical

and economic advantages of reducing the number of diffusion barrier layers and corresponding deposition steps from N (in prior art methods) to one. This results in a significant interconnect process simplification and chip manufacturing cost reduction.

A further technical advantage of the present invention is its compatibility with and applicability to various types of interconnect metallization materials. This includes metals such as copper, gold, silver, aluminum, and various superconducting materials.

Compatibility with damascene (single damascene and dual-damascene) interconnect fabrication methods is also another technical advantage of the present invention. The present invention provides excellent thermal management and efficient heat dissipation removal capabilities.

Another technical advantage of the present invention is improved interconnect metal lead and plug conductances due to elimination of the need for all (but one) barrier layers (all via-level barrier layers can be eliminated).

The present invention provides the technical advantage of improved interconnect metallization electromigration lifetime due to homogeneous metallization structure with large-grain metal lines and contact/via plugs as well as direct, i.e., barrierless plug-to-metal line contacts between the via plugs and the adjacent metal lines on different interconnect levels.

The present invention further provides the technical advantage of eliminating the need to use low-k dielectric materials and the relatively complex and expensive process integration methods associated with them. The present

invention reduces the number of fabrication process steps per interconnect level by about four steps, as compared to prior art methods for forming damascene interconnect structures with advanced low-k dielectrics.

This invention also provides the technical advantage of a much improved chip reliability by eliminating the physical paths for diffusion of the metal atoms, such as copper or gold or silver into the active semiconductor devices. Moreover, the free-space ILD/IMD structure eliminates the possibility of ILD/IMD electrical breakdown field degradation due to metal atom diffusion into the insulating regions. This eliminates the need for the use of diffusion barrier layers to encapsulate the metallization structure at each interconnect level.

The present invention provides the technical advantage of hermetic sealing of the multi-level interconnect structure and semiconductor IC devices either under vacuum or with the interconnect structure free-space medium filled and hermetically sealed with a controlled pressure of a suitable gas such as an inert gas (e.g., helium or argon).

Still a further technical advantage of the present invention is excellent mechanical strength and integrity of the multi-level interconnect structure and overall semiconductor chip resulting from the inventive process.

The present invention provides yet another advantage by uses a disposal interlevel/intermetal filler material during manufacture that is an electrically conductive or semi-conductive material that helps overcome damage to the

device that can occur through plasma charging during manufacture.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present invention and advantages thereof may be acquired by reference to the following description taken in conjunction with the accompanying drawings in which like reference numbers indicate like features and wherein:

FIGURE 1 illustrates the formation of a damascene trench in conjunction with an organic low-k dielectric layer according to a prior art method;

FIGUREs 2a and 2b shows two different inlaid copper interconnect lines with and without a conductive barrier layer;

FIGUREs 3a and 3b shows two different copper via plugs, one with a barrier layer, the other without a barrier layer, making electrical connections between two metal lines located on two different interconnect levels;

FIGUREs 4 and 5 depict exemplary prior art processes for preparing a dual-damascene multi-level copper interconnect structure;

FIGURE 6 is a process flow for one embodiment of the present invention (example shown for formation of a multi-level copper interconnect structure with free-space dielectric medium);

FIGURE 7 provides an alternative process flow for another embodiment of the present invention, different in some respects to that of FIGURE 6 (again example shown for

formation of a multi-level copper interconnect structure with free-space dielectric medium);

FIGURE 8 shows a multi-level interconnect structure formed as part of the process of the present invention (interconnect structure shown prior to completion of the final process steps for formation of free-space medium and hermetic sealing of the IC chips);

FIGUREs 9 through 12 show alternative embodiments of the top layer etchant transmission openings or windows for fabrication of the free-space dielectric interconnect structure of the present invention. FIGURE 9 shows an array of square shaped holes. FIGURE 10 shows an array of circular holes. FIGUREs 11 and 12 show two different arrays of rectangular-shaped holes.)

FIGURE 13 depicts the interconnect structure of FIGURE 8 following formation of the etchant-transmission window pattern on the top layer and after formation of the free-space dielectric medium for the purposes of illustrating one example of forming the free-space dielectric interconnect structure of the present invention;

FIGURE 14 shows the top dielectric layer after formation of the etchant transmission windows used to enable formation of the free-space dielectric medium, and also following the subsequent deposition steps for hermetic sealing of the interconnect structure of the present invention; and

FIGURE 15 shows the multi-level interconnect structure of the present invention after formation of the free-space dielectric medium, hermetically-sealed top layer, and the bonding pad windows.

BRIEF DESCRIPTION OF THE INVENTION:

FIGURE 4 shows one example of a prior art interconnect process flow 40 that results in a dual-damascene multi-level copper metallization interconnect structure in conjunction with inorganic interlevel dielectric (ILD) and intermetal dielectric (IMD) layers (e.g., fluorinated oxide or $Si_xO_yF_z$ ILD/IMD material). In this example, tungsten is used to form tungsten contact plugs (to keep copper away from silicon) while copper is used for all the via plugs. The interconnect fabrication process (or back-end-of-the-line or BEOL process) flow starts after completion of the front-end-of-the-line (FEOL) process flow utilized for fabrication of the transistor and isolation (and other devices such as diodes, capacitors, etc.) structures, as step 42 indicates.

The first ILD layer (ILD1) which may be SiO_2, $Si_xO_yF_z$, or another material) is deposited, as shown in step 44, by thermal CVD or PECVD and then globally planarized by chemical-mechanical polishing (CMP) and cleaned after the CMP step at step 46. Subsequently, the complete ILD structure is formed by deposition using CVD or PECVD of an additional amount of the dielectric material (e.g., SiO_2, $Si_xO_yF_z$, or another suitable insulating material), as indicated in step 48. After formation of the contact holes by microlithography and reactive ion etching or RIE as shown in the liner/barrier layers (e.g. Ti/TiN) are formed by PVD and/or CVD (see step 50, step 52). Then the tungsten contact plugs are formed by blanket deposition of a tungsten layer to fill the contact holes (see step 54)

followed by tungsten CMP and post-CMP clean as shown in steps 54 and 56. The fabrication flow then continues by deposition of a relatively thick etch-stop layer (e.g. silicon nitride layer) followed by deposition of the second ILD layer (e.g., SiO_2 or $Si_xO_yF_z$). The metal-1 (first metal level) line trenches, for subsequent formation of inlaid metal-1 interconnects, are formed by microlithography patterning and RIE (with the thin Si_3N_4 etch-stop layer used for RIE process end-pointing) (step 60). Si_3N_4 is also removed from the bottom of trenches by RIE. The RIE step used for removal of the silicon nitride layer at the bottom of the trenches selectively removes the nitride layer and stops on ILD1

Then, the diffusion barrier layer (TiN, Ta, TaN, or another suitable material) is deposited either by CVD or PVD (e.g., to form a 150Å to 300Å barrier layer) (step 62). The inlaid metal-1 interconnect lines are then formed by depositing copper (by MoCVD, PVD, and/or plating) followed by subsequent metal CMP and post-CMP clean through steps 64 and 66. The following dual-damascene copper interconnect level is fabricated by depositing the intermetal dielectric (IMD) layer (e.g., a multi-layer dielectric comprising a thin silicon nitride dielectric barrier and etch-stop layer, followed by deposition of SiO_2, a thin Si_3N_4 etch-stop layer, and a top layer of silicon dioxide (SiO_2) layer; the oxide layers may be replaced by a reduced-permittivity material such as $Si_xO_yF_z$), as shown in step 68. Then, a microlithography patterning process and a reactive ion etch (RIE) process sequence is used (step 70) in order to form the dielectric

trenches for subsequent formation of inlaid copper metal lines.

A follow-on microlithography patterning and dielectric RIE process sequence is used to form the interconnect via holes (step 72). Then, a diffusion barrier layer (TiN, Ta, TaN, etc.) is deposited by CVD or PVD, (step 74). Subsequently, a copper layer is deposited, as shown in step 78, (by MOCVD, PVD and/or Plating) and polished back by CMP, followed by post-CMP clean (step 80) resulting in formation of the embedded copper via plugs and inlaid metal interconnect lines. The repetitive steps of IMD deposition, microlithograrahy patterning and dielectric RIE processes (for via holes and interconnect metal line trenches), as well as barrier and copper deposition steps, and CMP and post-CMP clean are performed multiple times until all the necessary interconnect levels are fabricated, as verified at step 82. Then, the passivation overlayer (e.g., Si_3N_4 or SiON) is deposited by PECVD, at step 84. A microlithography patterning step and an RIE process step are used (step 86), to form the bonding pad openings or windows. The chip can then be packaged, as step 88 indicates.

The process flowchart 90 of FIGURE 5 presents another example of a state-of-the-art prior art interconnect process technology for formation of dual-damascene copper metallization with advanced low-k (e.g., $K \leq 2.5$) IMD/ILD layers. Process flow 90 is fairly similar to the prior art process flow of FIGURE 4 except for additional process steps 92 and 94. The additional process steps 92 and 94 for integration of copper and low-k dielectrics are

required in order to maintain good low-k dielectric integrity through the BEOL interconnect process flow and also to eliminate any process integration issues in terms of patterning and etch processes as well as any material compatibility issues. The description of the process flow outlined in FIGURE 5 is essentially similar to that already provided for the flowchart in FIGURE 4. One difference is that a thin layer of a hard mask material (such as SiO_2) is used to protect the ILD or IMD low-k dielectric surface prior to any patterning and CMP process steps.

Most of the organic low-k dielectric materials may be damaged in typical plasma ash processes used for removal of the patterned photoresist layers after patterning and etch processes (thus, the reason for the use of an oxide hard mask). Moreover, many low-k organic dielectrics may not be directly exposed to the CMP pad and slurry due to possible damage or degradation of their properties. This is another reason for using the oxide hard mask to protect the low-k dielectric. Moreover, this process flow forms a thin layer of dielectric (e.g., oxide) liner on the sidewalls of the dielectric trenches and via holes in order to protect a low-k dielectric from plasma etching and also to provide a good sidewall surface for deposition of the barrier layer. For IMD layers, the multi-layer stack comprises Si_3N_4, low-k dielectric, thin SiO_2, low-k dielectric, and thin SiO_2.

The lower and upper low-k dielectric layers house the via plugs and the inlaid interconnect metal lines on each level, respectively. The lower silicon nitride layer (thin nitride) is used as a dielectric diffusion barrier to encapsulate the lower level copper interconnect lines. The

middle thin SiO_2 layer is used as an etch-stop layer during the formation of the metal trenches. A comparison of process flow 40 of FIGURE 4 with process flow 90 of FIGURE 5 indicates that integration of advanced low-k dielectric materials (such as organic low-k materials) results in added process complexity and increased IC fabrication cost compared to standard silicon dioxide IMD material or its related materials (such as fluorinated oxide).

The following discussion focuses on the description of the interconnect process flows and structures of the present invention appearing in FIGUREs 6 and 7. Two closely related preferred flows of invention (preferred process flow embodiments) are shown in the flowchart 100 of FIGURE 6 and flowchart 150 of FIGURE 7. First, the description focuses on the process flow 100 of FIGURE 6. The back-end-of-the-line (BEOL) interconnect process flow starts after completion of the front-end-of-the-line (FEOL) fabrication process flow for the transistors, isolation regions, etc. (step 102). The next step is to deposit a blanket layer of a suitable dielectric diffusion barrier material which is also highly resistant against typical etch chemistries (e.g., HF-based etchants) used for oxide etching. For instance, it is possible to preferably deposit a layer of silicon nitride (e.g., 2000Å to 5000Å Si_3N_4) using thermal CVD, PECVD, or PVD (step 104). This layer will serve as a dense etch-resistant layer used for protection of the active transistor devices and isolation structures during subsequent etching of the disposable inter-level and inter-metal oxide layers. Moreover, this thick and dense etch-resistant dielectric barrier layer prevents any copper

diffusion into the silicon substrate and active device regions during the BEOL interconnect processing. Other suitable dielectric materials (e.g., AlN or diamond-like carbon or DLC) may be used instead of Si_3N_4 for this material layer.

After the blanket dielectric deposition process, the first disposable interlevel/intermetal filler material ($ILFM_1$) layer is deposited (step 106). The disposable interlevel/intermetal filler material is preferably an electrically conductive material, but can also be an electrically semi-conductive material. The disposable filler material should have an electrical resistivity preferably less than 10,000 microohms*centimeters (the filler material must have some level of electrical conductivity). Preferable filler materials can be easily deposited and etched away. The disposable filler material can be, for example, amorphous silicon, polycrystalline silicon, amorphous germanium, polycrystalline germanium, tin, and any alloy of amorphous silicon, polycrystalline silicon, amorphous germanium, polycrystalline germanium, and tin. As necessary, a dopant, such as boron, phosphorous, antimony or another suitable dopant, can be used to improve the electrical conductivity of the disposable filler material, including amorphous silicon. Each time a "filler material" is used in this disclosure, the filler material is the electrically conducting or semiconducting filler material described here, which is preferably amorphous silicon.

Thus, step 106 involves preferably depositing an amorphous silicon layer (preferably by physical vapor

deposition, but it could also be deposited by CVD or PECVD), thereby forming the first disposable interlevel filler material layer ($ILFM_1$). By using an electrically conducting filler material in each disposable layer during the manufacture of the interconnect structure, the risk of damage to the underlying device(s) is reduced. When using an insulating disposable dielectric material, the risk of damaging the underlying devices is greatly increased. By using an electrically conductive disposable filler material according to the present invention, during the etch of the plugs and/or trenches, the etch is into an equi-potential plane (which is non-insulating) the plasma induced damage (due to the charging effect) is greatly reduced or eliminated.

Next, dielectric CMP and post-CMP cleaning processes are performed (step 108) to form a globally planarized dielectric surface. This will provide a globally planar wafer surface throughout the multilevel interconnect fabrication process flow. Subsequently, a multi-layer disposable filler material stack (e.g., amorphous silicon/SiO_2/amorphous silicon) is deposited by CVD, PECVD, or PVD (step 110). This multi-layer disposable filler material stack can be formed using a dual damascene process. In the stack, the lower layer is for the via plugs and the upper layer is for the metal trenches.

The stack includes upper and lower amorphous silicon layers separated by a thin etch-stop (or etch end-point detection) layer of a different material, such as silicon dioxide (SiO_2) or aluminum oxide (Al_2O_3) or another suitable disposable material. To form a silicon dioxide etch stop

intermediate layer, a flash treatment of the first layer of the amorphous silicon in-situ with oxygen could be performed to form 10-50 angstroms of silicon dioxide, then the second amorphous silicon layer can be formed on top of the etch stop layer using a PVD process. This relatively thin intermediate etch stop layer will be used as an etch end-point marker during subsequent formation of the metal line trenches by anisotropic reactive-ion etching.

After deposition of the multi-layer disposable electrically conducting filler material stack, a microlithography patterning process and subsequent dielectric RIE (anisotropic etching) process are performed, as shown at step 112, to form the contact holes. Then, another microlithography patterning process and an anisotrophic RIE process are used to form the dielectric trenches for the first level of metal interconnect lines (step 114). Next, the first level metallization is performed by sequential deposition of the barrier layer (e.g., Ta, TaN, WN_x, or TiN by PVD or CVD) as shown in step 116, and a copper layer (by MoCVD, PVD, and/or plating), as indicated in step 118. Then, copper CMP and post-CMP clean processes are performed (step 120), in order to form the embedded copper contact plugs and inlaid metal lines.

Next, fabrication of the next interconnect level proceeds by deposition of a suitable multi-layer disposable filler material stack, preferably SiO_2/amorphous Si/SiO_2/amorphous Si formed by CVD, PECVD, or PVD (shown at step 122). The silicon oxyide (SiO_2) layers are relatively thin compared to the upper and lower amorphous silicon layers (e.g., 100Å to 500Å) and are used as etch-stop

layers during subsequent RIE etch processes for formation of the via holes and metal line trenches. Other suitable materials such as aluminum oxide may be as etch-stop layers. After the multi-layer stack deposition, two sequential steps of microlithography patterning and anisotropic RIE processes (steps 124 and 126) are performed for formation of the via holes and the interconnect metal line trenches. Next, a layer of copper is deposited (step 128), by MOCVD, PVD, and/or plating to fill the via holes and interconnect metal line trenches. Note that at this stage copper can be deposited directly on the patterned structure without a need for a diffusion barrier layer, thus, simplifying the interconnect process flow. If desired or necessary, an adhesion promotion glue layer may be deposited on the surface prior to deposition of copper.

Subsequently, copper CMP and post-CMP clean processes are performed, at step 130, in order to form the embedded via copper plugs and inlaid interconnect metal lines. The repetitive steps of multi-layer dielectric stack deposition, fabrication of via holes and metal line trenches, copper deposition, and copper CMP (and post-CMP clean) are performed multiple times until all the necessary interconnect levels are fabricated, as verified at step 132. After formation of all the necessary interconnect levels, a top etch-resistant dielectric layer, preferably a silicon nitride layer (on the order of 2000Å to 1 μm thick), is deposited by CVD, PECVD, or PVD, at step 134. Other suitable etch-resistant (and preferably high-thermal-conductivity dielectric materials) such as aluminum nitride or diamond-like carbon (DLC) may also be used instead of

silicon nitride. The schematic diagram of FIGURE 8 illustrates the example of a cross-sectional view of a multi-level interconnect structure (shown with six levels of copper interconnect) at this stage in the interconnect fabrication process flow.

Next, a microlithography patterning process and a subsequent anisotropic RIE process are performed (see step 136) in order to form etchant transmission windows or openings within the top dielectric layer. The schematic diagrams on pages FIGUREs 9, 10, 11 and 12 show several possible layout patterns of the etchant transmission windows, formed within the top etch-resistant layer. Preferably, the etchant transmission window pattern comprises openings or windows (squares, rectangular, circular, etc.) with at least one minimum-geometry in-plane dimension. For instance, the pattern of FIGURE 9 shows an array of closely-spaced square windows. For a 0.18 μm technology node, these windows may have 0.18μm x 0.18μm areas and the adjacent windows may be separated by 0.18μm. The alternative pattern in FIGURE 10 comprises an array of circular holes. Again, the holes may have minimum-geometry diameters (e.g., 0.18 μm diametric dimensions for circular holes separated by 0.18 μm from each other in a 0.18μm technology). FIGUREs 10 and 11 show two alternative etchant transmission window patterns comprising rectangular windows with larger overall transmission window area ratios (ratio of total area of the windows to the total surface area). The smaller side dimensions of these rectangular windows are preferably the same as the resolution of the microlithography tool (e.g., 0.18μm for a 0.18μm

technology), while the larger side dimensions (lengths of rectangular windows) may be several to tens to even hundreds of microns (μm). The idea is to have an etchant transmission window pattern which provides a relatively large transmission area ratio (preferably ≥ 50%) and can be subsequently hermetically sealed using a simple deposition process without a significant impact on the interconnect metallization structure. Preferably, the thickness of the top etch-resistant layer (e.g. Si_3N_4 or AIN layer deposited by CVD, PECVD, or PVD or any other vapor deposition process) is several times larger than the smaller side dimension of the etchant transmission unit cells. For instance, for a 0.18μm technology, we may use a 0.70 μm-to-1 μm thick silicon nitride top etch-resistant layer with etchant transmission window cells (square, circular, rectangular, or any other shape) which have 0.18 μm minimum in-plane dimension (e.g., rectangular unit cells, with 0.18 μm X 5 μm window size).

Returning to FIGURE 6, a highly selective etch process (preferable a dry etch process such as an isotropic dry etch in a halogen (e.g., SF_6) plasma, (although a wet etch process could be used) is performed at step 138 in order to selectively remove the entire multi-level disposable silicon dioxide dielectric structure. This etch chemistry and the resulting etch byproducts easily pass through the etchant transmission windows (or unit cells) facilitating the etch process. Due to the high packing density of the transmission unit cells and their relatively large area ratio, the selective etchant can easily remove the entire multi-level stack bound between the lower etch-resistant

layer (e.g., silicon oxide or aluminum nitride or DLC) and the upper etch-resistant patterned (e.g., also silicon oxide, aluminum nitride, or DLC) layer. The selective etchant (e.g., an SF_6-based dry etchant) does not or should not attack the metallization structure and may remove only a very small fraction of the top and bottom etch-resistant layers (e.g., silicon oxide, aluminum nitride, or DLC).

In general, the preference is to use an etchant with sufficiently high selectivity (>100:1) to the disposable ILD/IMD materials compared to the etch-resistant material which limits the thickness removal of the top and bottom etch-resistant layers (e.g., silicon oxide or aluminum nitride or DLC or another suitable dielectric) to preferably <1000Å. The schematic cross-sectional diagram of FIGURE 13 shows the resulting device structure after the selective removal of the disposable oxide dielectric layers. As shown, the multi-level copper interconnect structure is now surrounded by free-space medium within the structure between the top and bottom etch-resistant (e.g., silicon nitride) layers. The multi-level copper interconnect structure is mechanically supported by its own line and plug interconnections as well as the top and bottom boundary planes defined by the top and bottom etch-resistant silicon nitride layers which have sealed contacts to the top metal level and bottom contact plugs, respectively. If desired, a plurality of metallic columns made of stacked dummy contact and via plugs may be used to provide additional mechanical support between the top and bottom etch-resistant layers (this is optional but not necessary.)

At this stage, it is possible to perform an optional thermal anneal as shown at step 140 (e.g., at a temperature between 250°C and 400°C) in order to form large grains and preferred highly oriented texturing in the interconnect structure for improved electromigration lifetime, and enhanced metallization conductivity as well as to relieve any residual stresses. This optional thermal anneal process may also be used to form a large-grain multi-level copper metallization system with "bamboo-type" microstructure for maximum electromigration lifetime reliability improvement.

Next, the process flow continues with at least one deposition process and preferably two sequential material deposition process steps, as indicated at step 142. The first deposition process is a substantially conformal (CVD or PECVD) deposition process for deposition of a controlled thickness (e.g., 50Å to 200Å) of a dielectric material such as SiO_2, Si_3N_4, AlN, Al_2O_3, etc. The preferred material is silicon dioxide. This conformal deposition process deposits a thin (e.g., 50Å to 200Å) layer of encapsulating dielectric material such as SiO_2 over all the exposed surface areas of the multi-level metallization structure (metal lines and plugs). This deposition process also deposits a thin layer of the conformal dielectric over the exposed surfaces of the top etch-resistant patterned dielectric (e.g., silicon nitride), including the etchant transmission windows as well as a thin layer over the bottom etch-resistant layer. The amount of conformal dielectric thickness can be deliberately chosen to be small enough such that it is not sufficient to completely seal

the etchant transmission windows or the top patterned etch-resistant insulator.

The main purpose of this conformal dielectric (e.g., silicon dioxide) deposition step is to prevent or suppress thermionic emission and/or low-voltage electrical breakdown between the adjacent intra-level and inter-level metal lines and/or plugs through the free-space medium. The second deposition step is preferably a substantially nonconformal or directional deposition step (with poor step coverage) used to form a hermetically-sealed top insulating passivation overlayer. For instance, either PVD (plasma sputtering) or nonconformal PECVD (or other processes such as jet-vapor deposition or laser ablation) can be used to deposit a layer comprising silicon nitride, aluminum nitride, silicon oxynitride, diamond-like carbon (DLC), boron nitride or any combination of them. Preferably, the deposited material has excellent diffusion barrier properties against ionic contamination and moisture, and also has a relatively high thermal conductivity. For instance, this nonconformal or directional deposition may involve an atmospheric deposition process (preferably a thermal CVD process with helium carrier gas or an atmospheric laser ablation deposition process using a suitable target material in an inert atmosphere) for deposition of silicon nitride, aluminum nitride, DLC, or another suitable material.

The schematic diagrams shown in FIGURE 14 show an example of the evolution of the top dielectric layer starting from a patterned layer comprising etchant transmission windows and ending as a hermetically-sealed

structure with fully sealed windows (the top and bottom figures show the cross-sectional diagrams of the top dielectric layer before and after the conformal/non-conformal dielectric deposition processes).

Another practical process sequence for the hermetic sealing of the interconnect structure is as follows: (i) perform an atmospheric low-temperature silicon dioxide deposition (partially conformal) step using SiH_4/N_2O in a helium carrier gas in order to deposit a thin layer of oxide on the metallization structure and to seal the etchant transmission windows; (ii) Deposit a layer of silicon nitride (or silicon oxynitride) as passivation overlayer (this may be a ~ 5000Å thick layer deposited by PECVD); (iii) Deposit a layer (e.g., 5000Å to over 1μm thick layer) of high-thermal conductivity insulating material, preferably aluminum nitride or DLC, by a suitable deposition process (preferably RF magnetron sputtering or PECVD). This exemplary process sequence results in complete hermetic sealing of the chip interconnect structure by re-producing a continuous top passivation layer. Moreover, this process sequence results in a helium-filled free-space intermetal/interlevel dielectric medium. The atmospheric helium free-space dielectric medium provides an excellent heat transfer medium within the multi-level interconnect structure; it also further suppresses any thermionic emission (resulting in electrical leakage currents) or gas breakdown effects due to the intra-level and inter-level voltages between the adjacent metal lines and conductive plugs.

The example above shows the typical process flow for formation of a hermetically-sealed continuous dielectric layer on the top in conjunction with a hermetically sealed helium-filled (e.g., at or near atmospheric pressure) free-space interlevel/intermetal dielectric medium. If desired, the free-space helium pressure can be increased to above atmospheric pressure (e.g., 1 to 5 atmospheres) by performing the directional deposition (e.g., laser ablation) process (see FIGURE 14) in a pressurized process chamber filled with higher pressure helium. It is, however, emphasized that the preferred method and structure of this embodiment employ atmospheric or near-atmospheric helium (or another suitable inert gas such as argon) to fill the sealed free space interconnect dielectric ILD/IMD volume. Lower helium gas pressures (e.g., 1 Torr to 1 atm.) as well as other types of gas (e.g., argon, nitrogen, hydrogen, etc.) may be used to fill the free-space region.

A gas-filled free-space dielectric region is preferred over a near-vacuum free-space medium, both due to thermal management (efficient heat removal) and dielectric breakdown considerations. For instance, a helium-filled free-space medium 16 (preferably at or near atmospheric He pressure) provides a much superior heat transfer medium (in conjunction with the high-thermal conductivity copper metallization structure as well as the high-thermal-conductivity top and bottom etch-resistant layers), a superior breakdown-resistant interconnect structure, and a better thermionic-emission-resistant free-space medium compared to a vacuum free-space medium.

As indicated in the process flowchart of FIGURE 6, the next fabrication module is a microlithography patterning step (step 144), followed by an anisotropic dielectric RIE process in order to form the bonding pad windows by etching openings in the top passivation overlayer. The schematic diagram on FIGURE 15 shows the multi-level copper interconnect structure after this patterning and etch step. This structure includes multi-level copper interconnects bound between the bottom dielectric diffusion barrier layer and the top high-thermal-conductivity hermetic sealing layer. The metallization structure is surrounded by a sealed free-space medium filled with an inert gas such as helium.

Finally, the wafer is ready for dicing and packaging, at step 146 (such as flip-chip packaging). Note that the multi-level interconnect structure is fully hermetically sealed with an embedded free-space (preferably filled with He) ILD/IMD medium. This structure provides the highest level of interconnect electrical performance and reliability lifetime far superior to any interconnect structure comprising other low-k dielectric materials.

The process flow of the preferred embodiment of the present invention employs one extra microlithography masking step for formation of the etchant transmission windows in the top etch-resistant layer. The process flow of FIGURE 6 shows that two separate masking steps are used for formation of the etchant transmission windows and the bonding pad windows (resulting in the need for one extra masking step).

Alternatively, as shown in the alternative process flow 150 of FIGURE 7, it is possible to reduce the number of microlithography masking steps by one, through combining the microlithography patterning steps for the etchant transmission windows and bonding pads.

Process flow 150 of FIGURE 7 is essentially similar to the first embodiment (shown in FIGURE 6) through the copper CMP and post-CMP cleaning processes for the last (topmost) level of copper interconnect, i.e. step 132. Next, the top etch-resistant dielectric layer (or multi-layer material stack) is deposited by CVD, PVD, and/or PECVD, at step 134. For instance, it is possible to deposit either a layer of dense silicon nitride (e.g., 5000Å to ~ 1μm thick) by PECVD and/or PVD, or a bi-layer of Si_3N_4/AlN (e.g., 5000Å to over 1μm silicon nitride followed by 5000Å to over 1 μm aluminum nitride) by PECVD and/or PVD. Then a microlithography patterning process and a subsequent anisotropic dielectric RIE process are performed sequentially to form the etchant transmission windows (corresponding to a suitable pattern such as one of those examples shown in FIGUREs 9-12), and also the bonding pad windows at step 152. Note that this masking step combines the layouts of the etchant transmission windows and the bonding pads into one microlithography mask.

Next, the disposable amorphous silicon filler material layers are selectively removed using a highly selective, preferably dry, etchant at step 138. This results in the multi-level interconnect structure with free-space ILD/IMD medium surrounding the interconnect structure. Next, the copper metallization structure is coated with a controlled

thin layer (e.g. 50Å to 200Å) of silicon dioxide (or silicon nitride or another preferably insulating material) and the interconnect structure is hermetically sealed using the multi-step (e.g., two or three step) conformal/nonconformal dielectric deposition processes (step 142), as described in detail in association with FIGURE 6. The next fabrication process step is a blanket plasma (e.g., RIE) dielectric etch-back process until the bonding pads are re-exposed, at step 144.

This etch-back process, at step 144, can be easily endpointed using an optical etch end-point detection method (e.g., laser reflectance endpoint). Finally, the wafer is diced into IC chips and the chips are packaged using a suitable packaging technology. Based on this alternative second embodiment of this invention, the total number of microlithography masking step for an N-level interconnect structure is 2N+1, which is the same as the number of masks required in conventional prior art interconnect process flows. The first embodiment of this invention (shown in FIGURE 6) employs 2N+2 microlithography masking steps.

Although the present invention has been described in detail, it should be understood that various changes, substitutions and alterations can be made hereto without departing from the spirit and scope of the invention as defined by the appended claims.

WHAT IS CLAIMED IS:

1. A multi-level interconnect structure for a semiconductor integrated circuit chip on a semiconductor substrate comprising:

a plurality of electrically conductive metallization levels, each of said metallization levels comprising a plurality of electrically conductive interconnect segments;

a plurality of electrically conductive plugs for electrically connecting between various metallization levels and between said metallization levels and a plurality of semiconductor devices;

a free-space medium occupying at least a substantial portion of the electrically insulating regions within said multi-level interconnect structure;

an electrically insulating top passivation overlayer for hermetic sealing of said multi-level interconnect structure and for protection of said integrated circuit chip, said top passivation overlayer also serving as a heat transfer medium for facilitating heat removal from said interconnect structure and providing additional mechanical support for said interconnect structure through contact with the top metallization level of said multi-level interconnect structure; and

a plurality of metallization trenches and a plurality of metalization vias, wherein the processes used to form metallization trenches and vias do not produce any plasma damage.

2. The multi-level interconnect structure of Claim 1 wherein at least a portion of said electrically conductive interconnect segments is made of copper.

3. The multi-level interconnect structure of Claim 1 wherein at least a portion of said electrically conductive plugs is made of copper.

4. The multi-level interconnect structure of Claim 1 wherein at least a portion of said electrically conductive interconnect segments and plugs is made of a material comprising silver or aluminum.

5. The multi-level interconnect structure of Claim 1 wherein at least a portion of said electrically conductive interconnect segments and plugs is made of a material comprising a superconducting material.

6. The multi-level interconnect structure of Claim 1 wherein said semiconductor substrate is silicon, or silicon-on-insulator, or galium arsenide.

7. The multi-level interconnect structure of Claim 1 wherein said electrically insulating top passivation overlayer is made of a material comprising silicon nitride, silicon oxynitride, aluminum nitride, diamond-like coating, boron nitride or silicon carbide.

8. The multi-level interconnect structure of Claim 1 wherein said electrically insulating top passivation

overlayer comprises a material layer with a plurality of open bonding pad windows and closed resealed windows, the latter used for formation of said free-space medium and subsequent hermetic sealing of said interconnect structure.

9. The multi-level interconnect structure of Claim 1 wherein said multi-level interconnect structure is further supported by an electrically insulating bottom buffer layer, said electrically insulating bottom buffer layer separating said multi-level interconnect structure from underlying transistors and isolation regions fabricated within said semiconductor integrated circuit chip substrate.

9. The multi-level interconnect structure of Claim 1, wherein said hermetically sealed free-space medium comprises a gas.

10. A method for formation of a multi-level interconnect structure comprising the steps of:

fabricating a plurality of metallization levels, said metallization levels separated by and embedded within a disposable filler material layers;

fabricating a plurality of electrically conductive plugs in conjunction with said metallization levels and embedded within said disposable filler material layers;

depositing a top insulator layer over said plurality of metallization levels;

forming a plurality of openings within said top insulating layer;

selectively removing said disposable filler material layers to form a free-space dielectric medium surrounding at least a substantial portion of said plurality of metallization levels and said electrically a conductive plugs;

forming a hermetically-sealed interconnect structure with a free-space dielectric medium by depositing an electrically insulating material layer and sealing said plurality of openings without substantially shrinking the overall volume of said free-space dielectric medium; and

forming the bonding pad openings.

11. The method of Claim 10, wherein the disposable filler material is an electrically conducting material.

12. The method of Claim 10, wherein the disposable filler material is an electrically semi-conducting material.

13. The method of Claim 10, wherein the disposable filler material is an electrically conducting or semi-conducting material selected from the group of amorphous silicon, polycrystalline silicon, amorphous germanium, polycrystalline germanium, tin, and any alloy of amorphous silicon, polycrystalline silicon, amorphous germanium, polycrystalline germanium, and tin.

14. The method of Claim 10, further comprising:

positioning of each metallization layer by etching through the disposable filler material layer, wherein the disposable filler layer material is electrically conducting or semi-conducting to prevent damage to the devices.

15. The method of Claim 10, wherein at least a portion of said plurality of metallization levels and electrically conductive plugs is formed within said disposable filler material layers using a damascene process flow.

16. The method of Claim 10 wherein said multi-level interconnect structure is formed using 2N+1 microlithography masking steps for N metallization levels.

17. The method of Claim 10 wherein said multi-level interconnect structure is formed using 2N+2 microlithography masking steps for N metallization levels.

18. The method of Claim 10 wherein said disposable filler material layers comprise silicon oxide.

19. The method of Claim 10, further comprising the step of forming said multi-level interconnect structure to be supported by a bottom electrically insulating buffer layer, said electrically insulating bottom buffer layer separating said multi-level interconnect structure from underlying transistors and isolation regions fabricated within said semiconductor integrated circuit substrate.

20. The method of Claim 10, further comprising the step of forming said electrically insulating bottom buffer layer to provide additional mechanical support for said multi-level interconnect structure.

21. The method of Claim 20, further comprising the step of forming said electrically insulating bottom buffer layer to further provide a dielectric material with effective diffusion barrier properties against contamination of the semiconductor substrate by the contaminating metallization materials and external ionic contaminants.

22. The method of Claim 10, further comprising the step of forming said hermetically-sealed free-space medium to comprise a gaseous material.

23. The method of Claim 22, further comprising the step of forming said gaseous material to be in the pressure range of less than 5 atmospheres.

24. The method of Claim 22, further comprising the step of forming said gaseous material to be at or near atmospheric pressure.

25. The method of Claim 10, further comprising the step of forming said encapsulating layer to comprise an electrically insulating layer.

26. The method of Claim 10, further comprising the step of forming at least a portion of said plurality of

electrically conductive interconnect segments and plugs to comprise a high electrical conductivity material.

27. The method of Claim 26 wherein said high electrical conductivity material comprises copper, silver, gold, aluminum, or a superconducting material.

28. The method of Claim 26 wherein said high electrical conductivity material is deposited using chemical-vapor deposition, physical-vapor deposition, and/or electroplating.

29. The method of Claim 10, further comprising fabricating an etch stop layer between each disposable filler material layer.

30. The method of Claim 29, where the etch stop layers are an oxide or a silicon dioxide layer.

31. The method of Claim 29, wherein the etch stop layers are formed by interrupted deposition.

32. The method of Claim 31, wherein the interrupted deposition involves plasma oxidation.

33. The method of Claim 29, further comprising removing the disposable filler material layers is performed using a dry etch process.

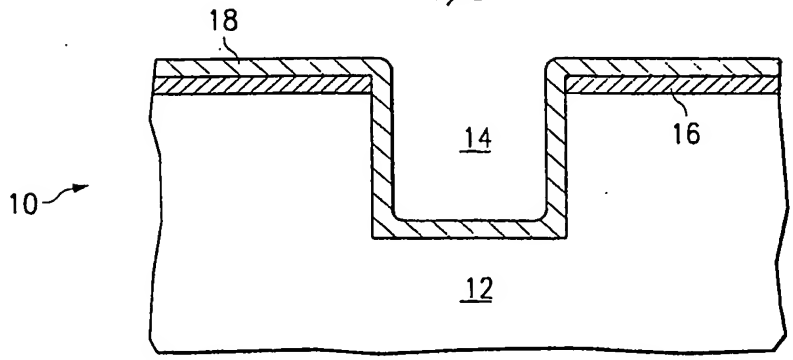


FIG. 1
(PRIOR ART)

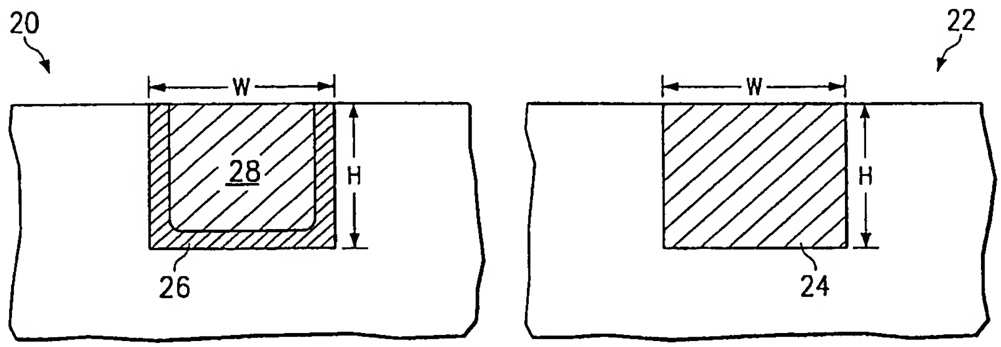


FIG. 2
(PRIOR ART)

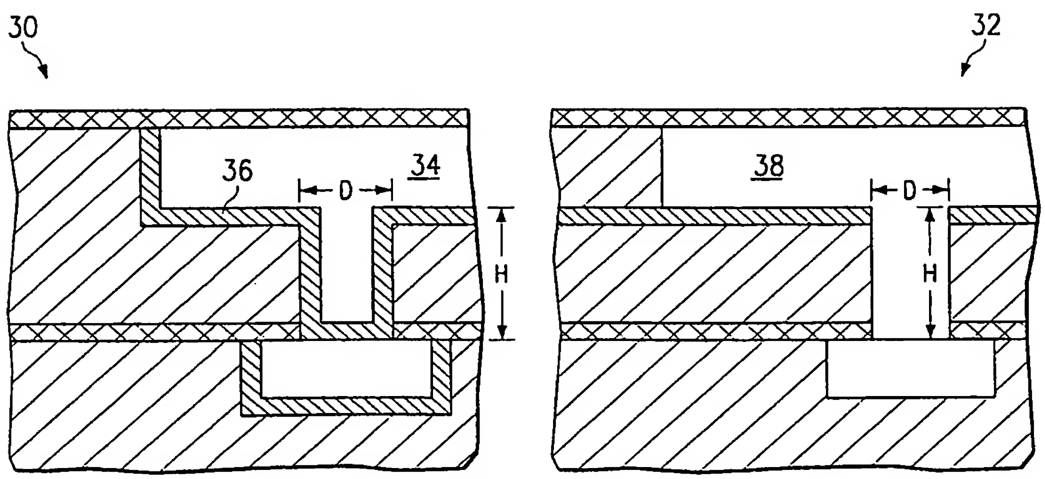


FIG. 3
(PRIOR ART)

2/9

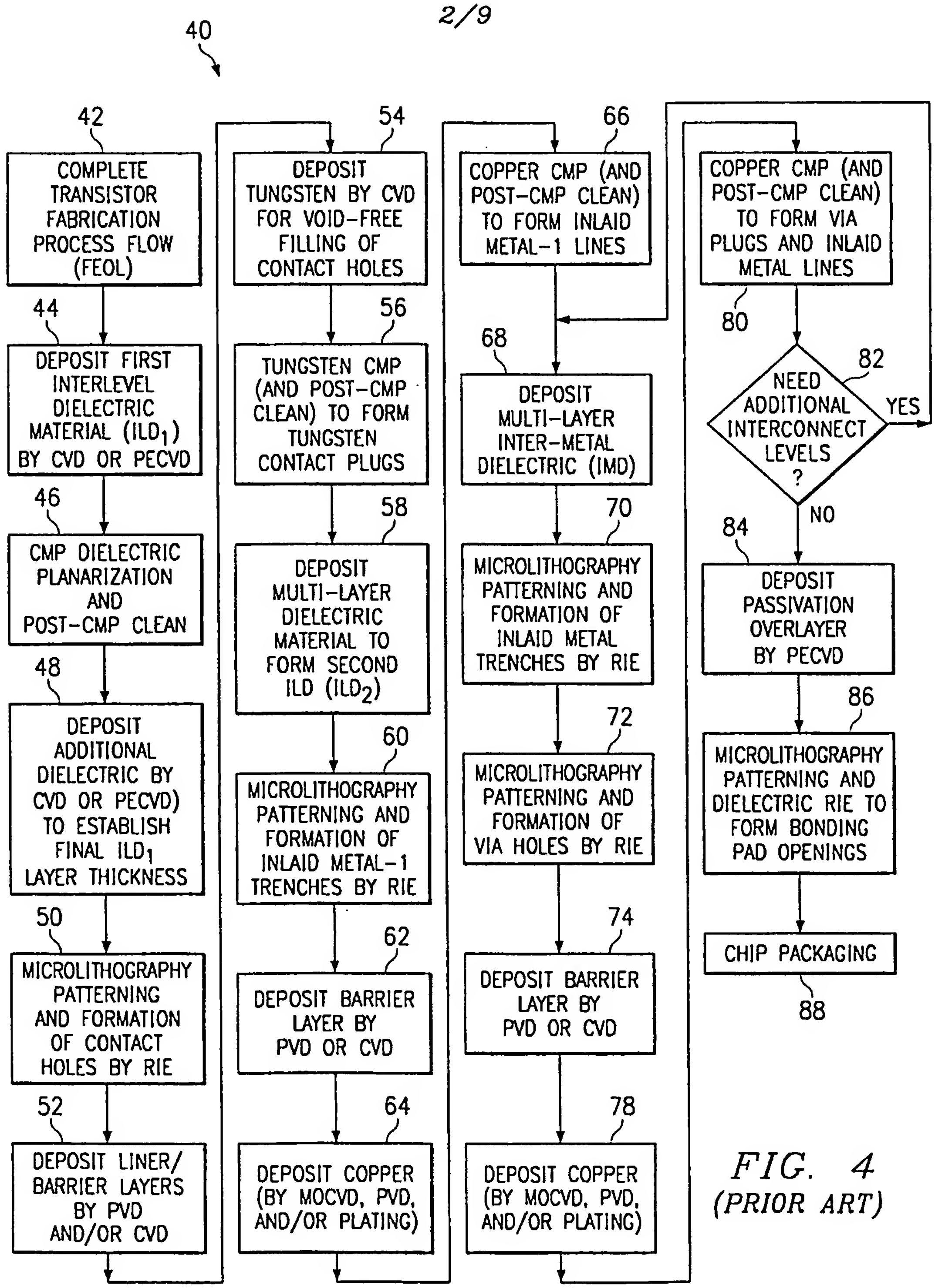
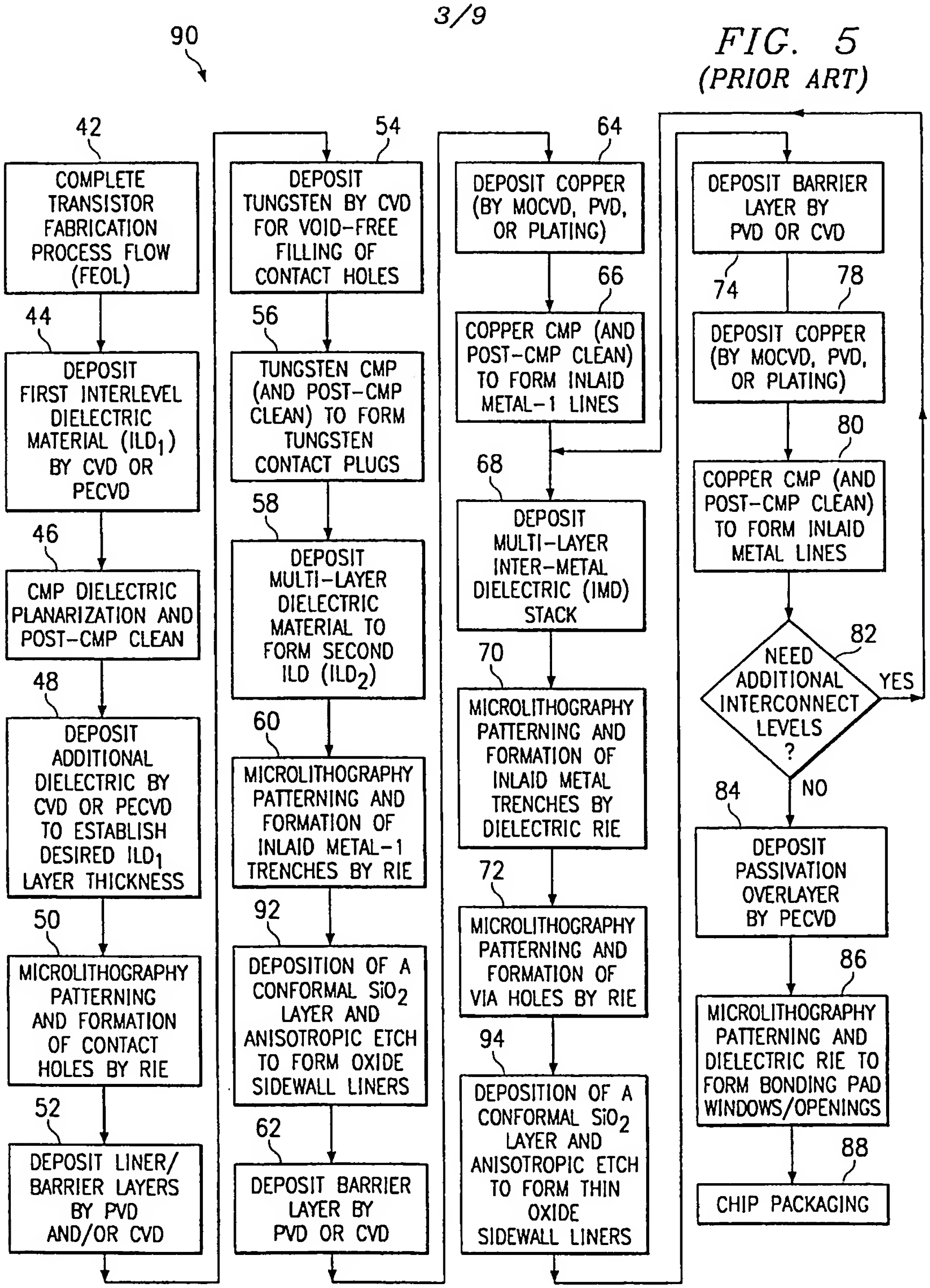
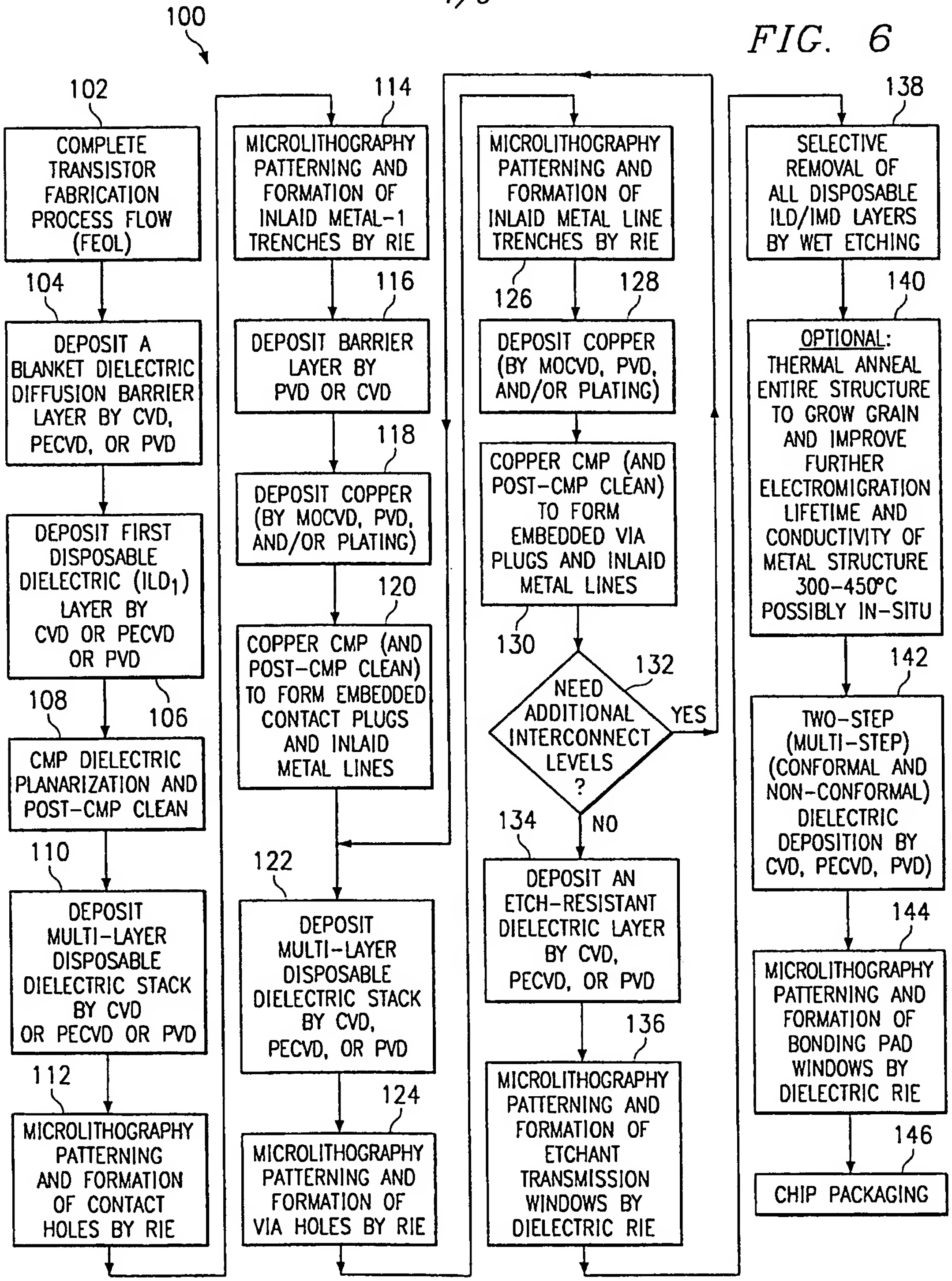


FIG. 4
(PRIOR ART)

FIG. 5
(PRIOR ART)



4/9



100
102
COMPLETE TRANSISTOR FABRICATION PROCESS FLOW (FEOL)
104
DEPOSIT A BLANKET DIELECTRIC DIFFUSION BARRIER LAYER BY CVD, PECVD, OR PVD
DEPOSIT FIRST DISPOSABLE DIELECTRIC (ILD1) LAYER BY CVD OR PECVD OR PVD
108
106
CMP DIELECTRIC PLANARIZATION AND POST-CMP CLEAN
110
DEPOSIT MULTI-LAYER DISPOSABLE DIELECTRIC STACK BY CVD OR PECVD OR PVD
112
MICROLITHOGRAPHY PATTERNING AND FORMATION OF CONTACT HOLES BY RIE
114
MICROLITHOGRAPHY PATTERNING AND FORMATION OF INLAID METAL-1 TRENCHES BY RIE
116
DEPOSIT BARRIER LAYER BY PVD OR CVD
118
DEPOSIT COPPER (BY MOCVD, PVD, AND/OR PLATING)
120
COPPER CMP (AND POST-CMP CLEAN) TO FORM EMBEDDED CONTACT PLUGS AND INLAID METAL LINES
122
DEPOSIT MULTI-LAYER DISPOSABLE DIELECTRIC STACK BY CVD, PECVD, OR PVD
124
MICROLITHOGRAPHY PATTERNING AND FORMATION OF VIA HOLES BY RIE
MICROLITHOGRAPHY PATTERNING AND FORMATION OF INLAID METAL LINE TRENCHES BY RIE
126
128
DEPOSIT COPPER (BY MOCVD, PVD, AND/OR PLATING)
COPPER CMP (AND POST-CMP CLEAN) TO FORM EMBEDDED VIA PLUGS AND INLAID METAL LINES
130
132
NEED ADDITIONAL INTERCONNECT LEVELS ?
YES
NO
134
DEPOSIT AN ETCH-RESISTANT DIELECTRIC LAYER BY CVD, PECVD, OR PVD
136
MICROLITHOGRAPHY PATTERNING AND FORMATION OF ETCHANT TRANSMISSION WINDOWS BY DIELECTRIC RIE
138
SELECTIVE REMOVAL OF ALL DISPOSABLE ILD/IMD LAYERS BY WET ETCHING
140
OPTIONAL: THERMAL ANNEAL ENTIRE STRUCTURE TO GROW GRAIN AND IMPROVE FURTHER ELECTROMIGRATION LIFETIME AND CONDUCTIVITY OF METAL STRUCTURE 300-450°C POSSIBLY IN-SITU
142
TWO-STEP (MULTI-STEP) (CONFORMAL AND NON-CONFORMAL) DIELECTRIC DEPOSITION BY CVD, PECVD, PVD)
144
MICROLITHOGRAPHY PATTERNING AND FORMATION OF BONDING PAD WINDOWS BY DIELECTRIC RIE
146
CHIP PACKAGING

FIG. 6

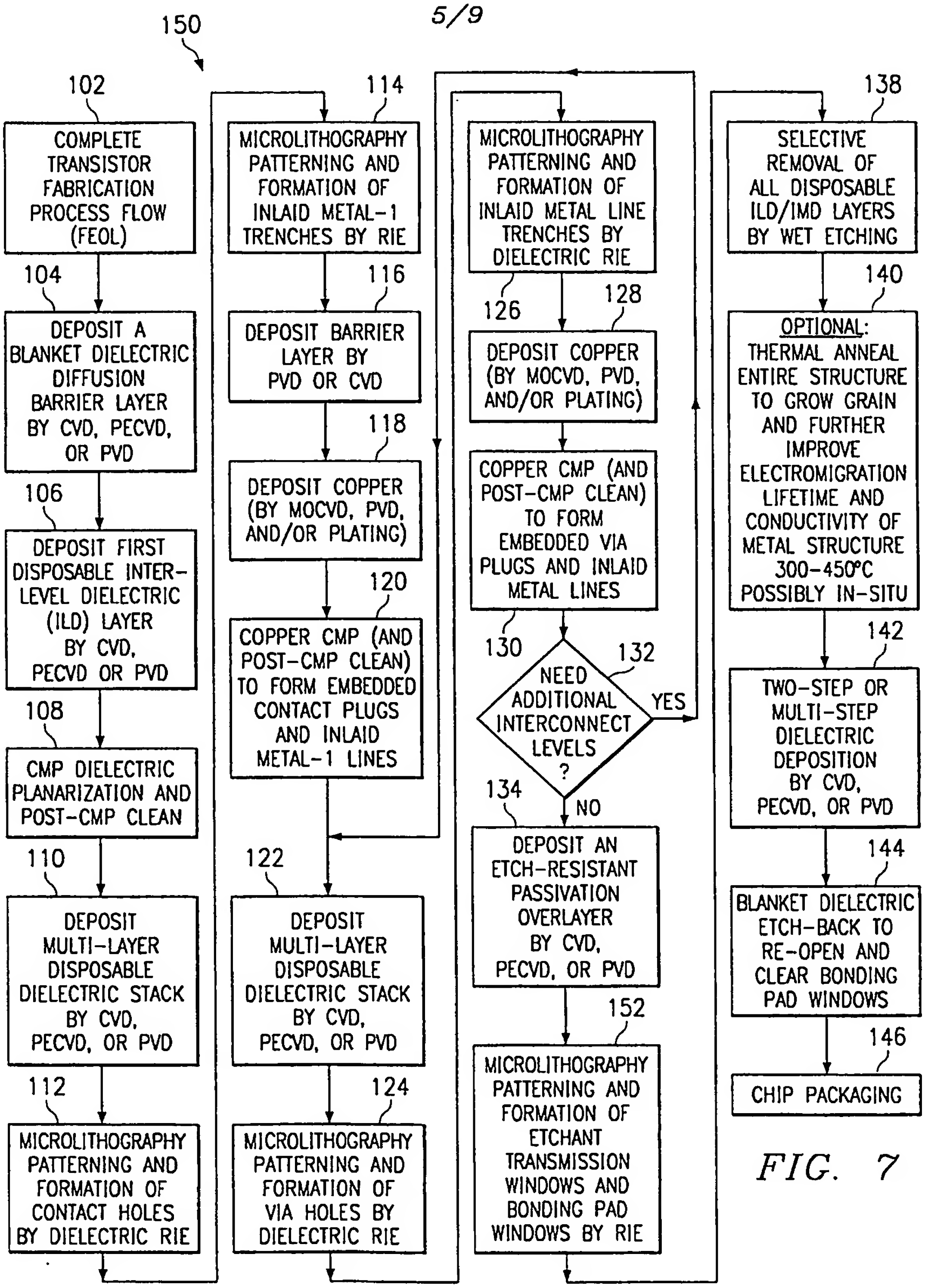

150
102
COMPLETE TRANSISTOR FABRICATION PROCESS FLOW (FEOL)
104
DEPOSIT A BLANKET DIELECTRIC DIFFUSION BARRIER LAYER BY CVD, PECVD, OR PVD
106
DEPOSIT FIRST DISPOSABLE INTER-LEVEL DIELECTRIC (ILD) LAYER BY CVD, PECVD OR PVD
108
CMP DIELECTRIC PLANARIZATION AND POST-CMP CLEAN
110
DEPOSIT MULTI-LAYER DISPOSABLE DIELECTRIC STACK BY CVD, PECVD, OR PVD
112
MICROLITHOGRAPHY PATTERNING AND FORMATION OF CONTACT HOLES BY DIELECTRIC RIE
114
MICROLITHOGRAPHY PATTERNING AND FORMATION OF INLAID METAL-1 TRENCHES BY RIE
116
DEPOSIT BARRIER LAYER BY PVD OR CVD
118
DEPOSIT COPPER (BY MOCVD, PVD, AND/OR PLATING)
120
COPPER CMP (AND POST-CMP CLEAN) TO FORM EMBEDDED CONTACT PLUGS AND INLAID METAL-1 LINES
122
DEPOSIT MULTI-LAYER DISPOSABLE DIELECTRIC STACK BY CVD, PECVD, OR PVD
124
MICROLITHOGRAPHY PATTERNING AND FORMATION OF VIA HOLES BY DIELECTRIC RIE
MICROLITHOGRAPHY PATTERNING AND FORMATION OF INLAID METAL LINE TRENCHES BY DIELECTRIC RIE
126
128
DEPOSIT COPPER (BY MOCVD, PVD, AND/OR PLATING)
COPPER CMP (AND POST-CMP CLEAN) TO FORM EMBEDDED VIA PLUGS AND INLAID METAL LINES
130
132
NEED ADDITIONAL INTERCONNECT LEVELS ?
YES
NO
134
DEPOSIT AN ETCH-RESISTANT PASSIVATION OVERLAYER BY CVD, PECVD, OR PVD
152
MICROLITHOGRAPHY PATTERNING AND FORMATION OF ETCHANT TRANSMISSION WINDOWS AND BONDING PAD WINDOWS BY RIE
138
SELECTIVE REMOVAL OF ALL DISPOSABLE ILD/IMD LAYERS BY WET ETCHING
140
OPTIONAL: THERMAL ANNEAL ENTIRE STRUCTURE TO GROW GRAIN AND FURTHER IMPROVE ELECTROMIGRATION LIFETIME AND CONDUCTIVITY OF METAL STRUCTURE 300-450°C POSSIBLY IN-SITU
142
TWO-STEP OR MULTI-STEP DIELECTRIC DEPOSITION BY CVD, PECVD, OR PVD
144
BLANKET DIELECTRIC ETCH-BACK TO RE-OPEN AND CLEAR BONDING PAD WINDOWS
146
CHIP PACKAGING

FIG. 7

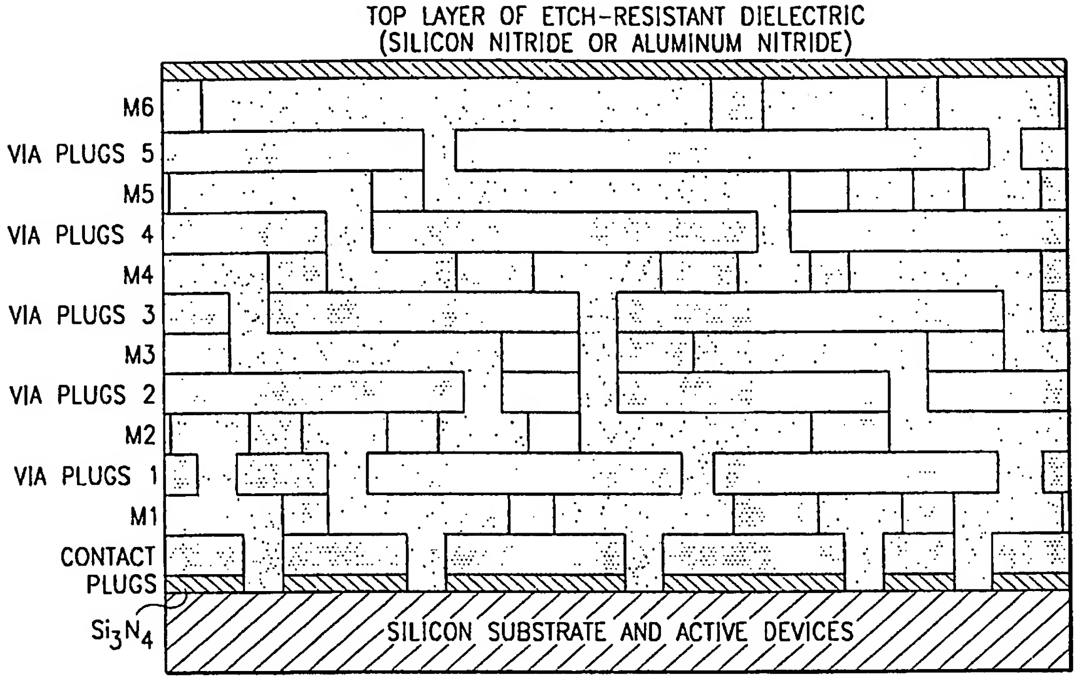

TOP LAYER OF ETCH-RESISTANT DIELECTRIC
(SILICON NITRIDE OR ALUMINUM NITRIDE)
M6
VIA PLUGS 5
M5
VIA PLUGS 4
M4
VIA PLUGS 3
M3
VIA PLUGS 2
M2
VIA PLUGS 1
M1
CONTACT PLUGS
Si_3N_4
SILICON SUBSTRATE AND ACTIVE DEVICES

FIG. 8

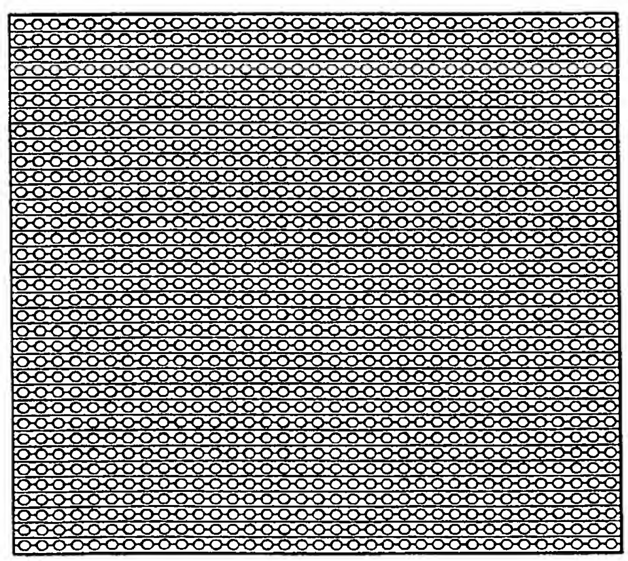


FIG. 9

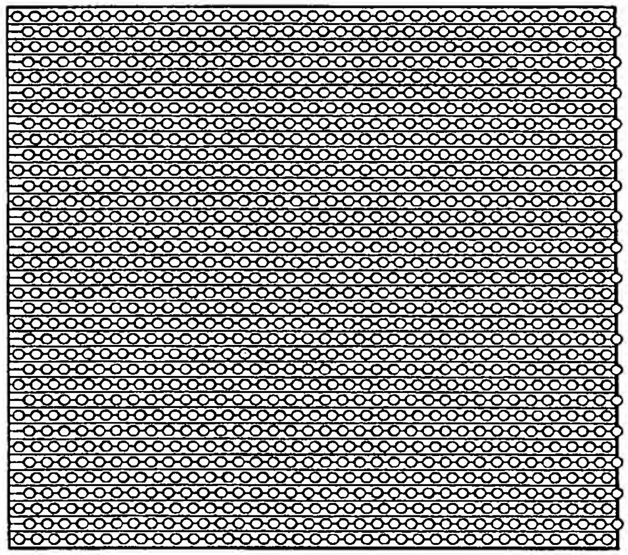


FIG. 10

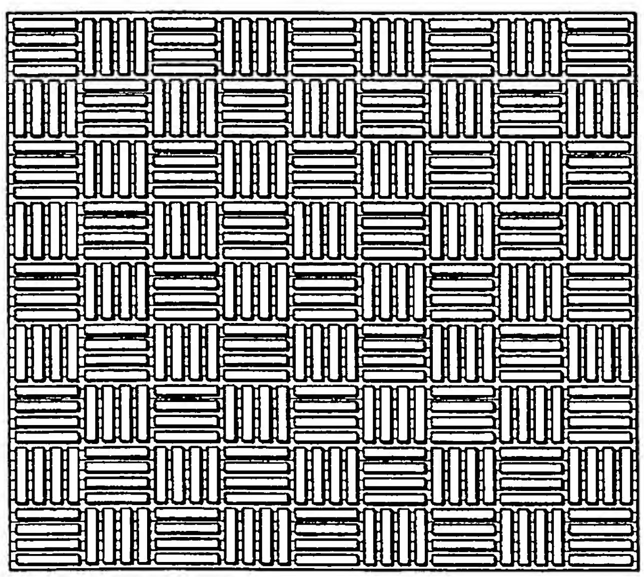


FIG. 11

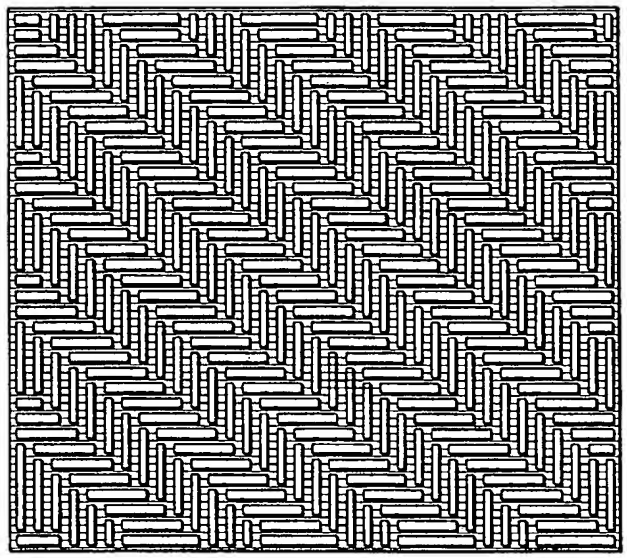


FIG. 12

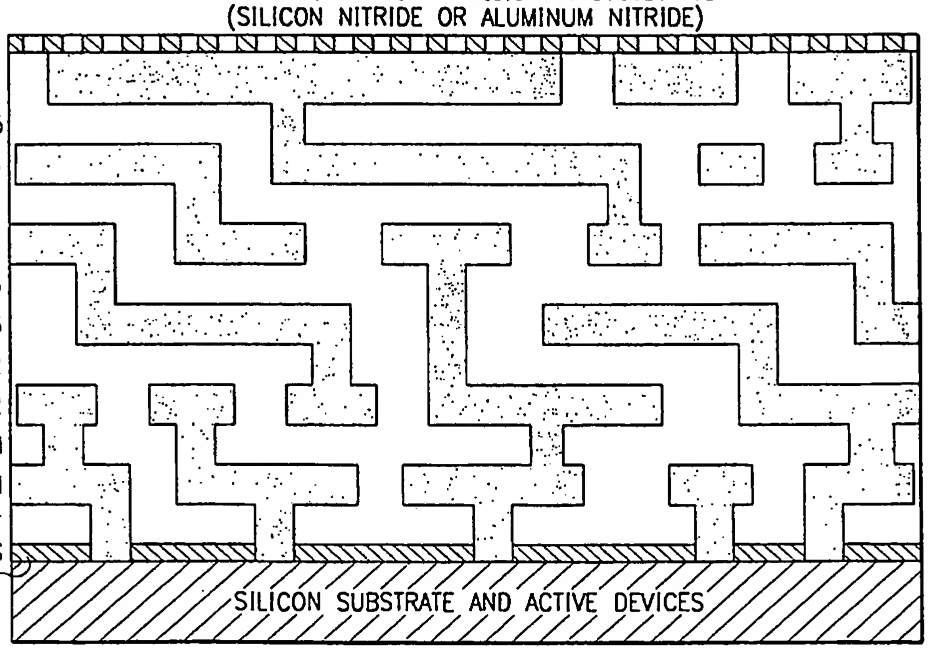

TOP LAYER OF ETCH-RESISTANT DIELECTRIC
(SILICON NITRIDE OR ALUMINUM NITRIDE)
M6
VIA PLUGS 5
M5
VIA PLUGS 4
M4
VIA PLUGS 3
M3
VIA PLUGS 2
M2
VIA PLUGS 1
M1
CONTACT PLUGS
Si_3N_4
SILICON SUBSTRATE AND ACTIVE DEVICES

FIG. 13

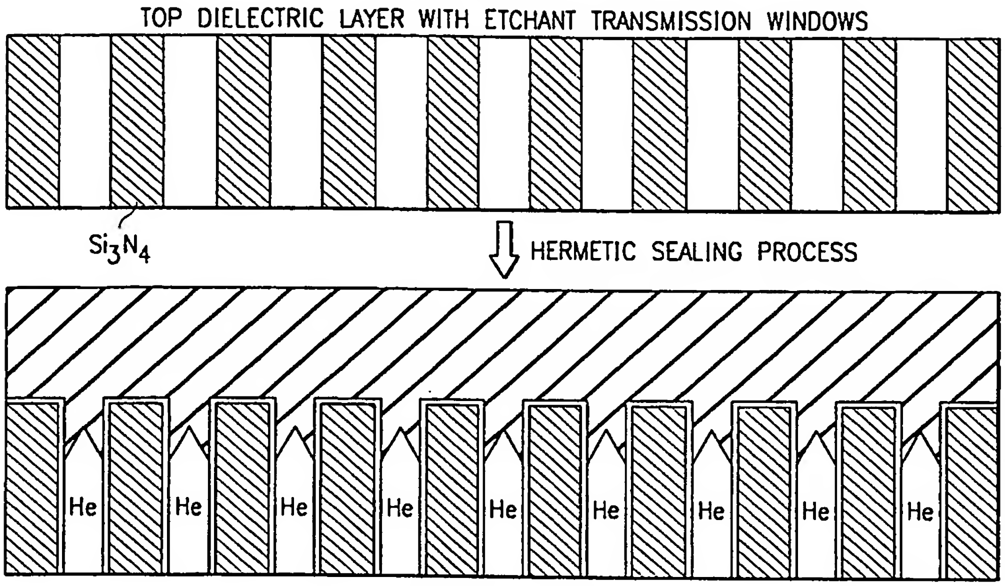

TOP DIELECTRIC LAYER WITH ETCHANT TRANSMISSION WINDOWS
Si3N4
HERMETIC SEALING PROCESS
He

FIG. 14

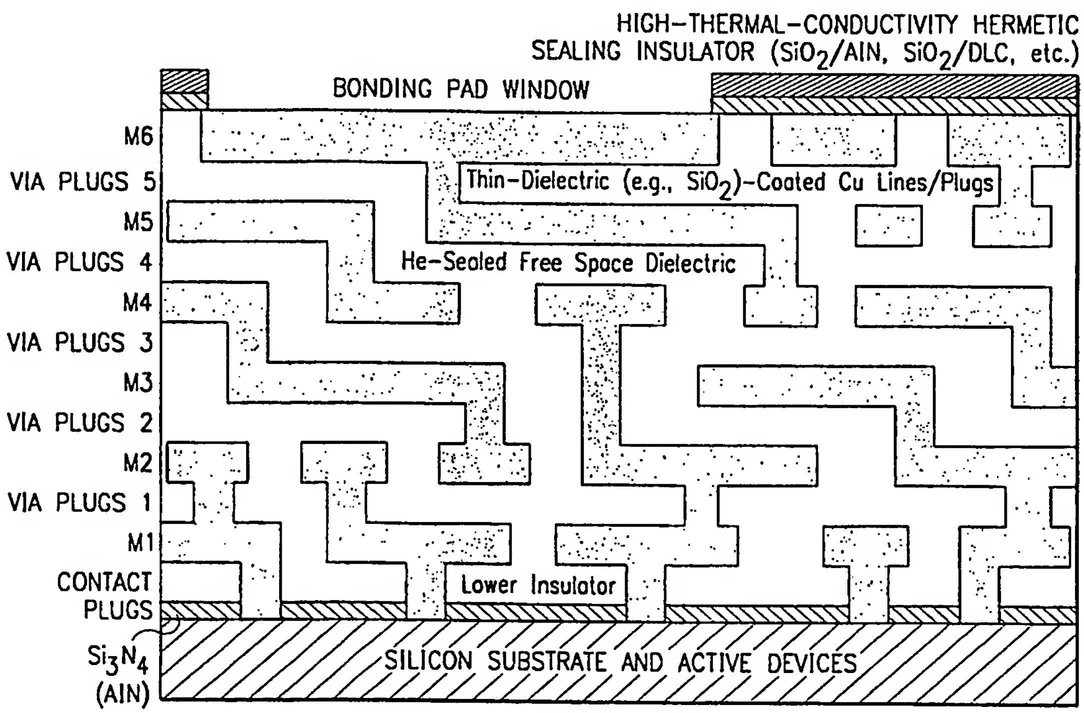

HIGH-THERMAL-CONDUCTIVITY HERMETIC SEALING INSULATOR (SiO2/AIN, SiO2/DLC, etc.)
BONDING PAD WINDOW
M6
VIA PLUGS 5
Thin-Dielectric (e.g., SiO2)-Coated Cu Lines/Plugs
M5
VIA PLUGS 4
He-Sealed Free Space Dielectric
M4
VIA PLUGS 3
M3
VIA PLUGS 2
M2
VIA PLUGS 1
M1
CONTACT PLUGS
Lower Insulator
Si3N4 (AIN)
SILICON SUBSTRATE AND ACTIVE DEVICES

FIG. 15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/28955

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) :H01L 21/44, 29/00
US CL : 257/522, 758, 759; 438/421, 619, 622, 634
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 257/522, 758, 759; 438/421, 619, 622, 634

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EAST, IEEE Transations
Search terms: dielectric constant, interconnection, multi-layer, air, space, superconductive

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 5,413,962 A (Lur et al) 09 May 1995 (09.05.95), col 2, lines 41-64	1-4, 6, 7, 9 ---- 5, 6, 8, 10-33
A, P	US 5,882,963 A (Kerber et al) 16 March 1999 (16.03.99), col 3, lines 55-66	1-33
Y	US 5,183,800 A (Nakagawa) 02 February 1993 (02.02.93), col 5, lines 29-35	5
X --- Y	US 5,372,969 A (Moslehi) 13 December 1994 (13.12.94), col. 2, lines 29-35	1-4, 7, 9 ---- 5, 6, 8, 10-33
Y	US 5,654,220 A (Leedy) 05 August 1997 (05.08.97), col. 12, lines 14-38	10-33

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
09 MARCH 2000	25 APR 2000

Name and mailing address of the ISA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	Tom Thomas
Facsimile No. (703) 305-3230	Telephone No. (703) 308-0956

Form PCT/ISA/210 (second sheet) (July 1998)★

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/28955

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4,561,173 A (Velde) 31 December 1985 (31.12.85), col. 7, lines 55-65	11